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Abstract

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TI An advanced technique for fabricating **hemispherical-grained** (HSG) silicon storage electrodes
AU Watanabe, Hirohito; Tatsumi, Toru; Ikarashi, Taeko; Sakai, Akira; Aoto, Nahomi; Kikkawa, Takamaro
CS ULSI Device Development Laboratories, NEC Corporation, Sagamihara, 229, Japan
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AB In this new fabrication technol. for high-d. DRAM's, an electrode with an even-surface amorphous-Si is changed to one with an uneven-surface **hemispherical-grained** Si (HSG-Si). This fabrication method consists of easily controllable processes: formation of smooth amorphous Si electrodes by low-pressure CVD followed by removal of native oxide and high-vacuum annealing. This annealing process can form HSG-Si covering the entire surface of all types of storage electrodes, including side-wall surfaces which had previously been dry-etched. The resulting storage electrode with HSG-Si can store 1.8 times as much charge as can be stored an electrode without HSG-Si. Such an increase makes it possible to reduce the height of storage electrodes. This technique is applicable to the fabrication of high-d. DRAM's.

An Advanced Technique for Fabricating Hemispherical-Grained (HSG) Silicon Storage Electrodes

Hirohito Watanabe, Toru Tatsumi, Taeko Ikarashi, Akira Sakai, Nahomi Aoto, and Takamaro Kikkawa, *Member, IEEE*

Abstract—**In this new fabrication technology for high-density DRAM's, an electrode with an even-surface amorphous-silicon is changed to one with an uneven-surface hemispherical-grained Si (HSG-Si). This fabrication method consists of easily controllable processes: formation of smooth amorphous Si electrodes by low-pressure chemical vapor deposition followed by removal of native oxide and high-vacuum annealing. This annealing process can form HSG-Si covering the entire surface of all types of storage electrodes, including side-wall surfaces which had previously been dry-etched. The resulting storage electrode with HSG-Si can store 1.8 times as much charge as can be stored an electrode without HSG-Si. Such an increase makes it possible to reduce the height of storage electrodes. This technique is applicable to the fabrication of high-density DRAM's.**

I. Introduction

THE miniaturization of DRAM structures has led to a reduction in cell area and, as a result, in cell capacitance. This reduced capacitance has caused a very serious limitation to further DRAM integration. The area allowed for a single cell in a 64-Mbit DRAM is about 1.4 μm^2 and it is difficult to provide a sufficient capacitance in such a limited area when using the conventional stacked capacitor, which has SiO_2/Si_3N_4 dielectric films. The development of a material with a higher dielectric constant is a promising solution to this problem [1], but when the Si_3N_4 dielectric film is combined with large-surface-area electrode techniques it is still the most practical capacitor dielectric material. A number of advanced storage electrode structures, including fin- and box-electrode type structures, have been studied, but although their storage capacitance is higher because their electrode surface areas are larger, their fabrication processes have been too complicated for mass-production [2]–[4].

A recent approach to increasing surface area has been the fabrication of uneven Si film surfaces. Low-pressure chemical vapor deposition (LPCVD) was used to produce a hemispherical-grained (HSG) Si surface, and has proved to be an efficient technique for enlarging the surface area [5]–[11]. Its application to DRAM processes, however, has involved significant difficulties, one of which is the strict temperature control required for depositing uniform LPCVD HSG-Si films [6]–[11]. Another is that after LPCVD HSG-Si formation, the excess HSG-Si between adjacent storage electrodes should be etched off to ensure electrical isolation. Then a smooth part appears at the foot of electrodes [8], [10]. It has recently been reported by Sakai *et al.* that Si films with an uneven surface morphology can be formed by amorphous Si deposition followed by *in-situ* annealing under ultrahigh vacuum [12], [13]. This uneven Si surface morphology is similar to that of the HSG-Si film deposited by LPCVD.

In the present work, we have developed a new technique in which the surface of a smooth amorphous-Si electrode without native oxide is changed into an uneven HSG-Si surface by a simple high-vacuum annealing [12]. With this technique, the surface area of any structural type of storage electrode can be increased by converting it to HSG-Si.

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H. Watanabe, N. Aoto, and T. Kikkawa are with the ULSI Device Development Laboratories, NEC Corporation, Sagamihara 229 Japan.

T. Tatsumi, T. Ikarashi, and A. Sakai are with the Microelectronics Research Laboratories, NEC Corporation, Tsukuba 305 Japan.

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II. Experiments

A. HSG-Si Formation

Two kinds of amorphous Si films were formed by Si molecular-beam deposition (MBD) and by LPCVD on SiO_2/Si substrates. The MBD amorphous Si films were deposited from electron-beam-evaporated Si using UHV molecular-beam epitaxy equipment with a base pressure of 1×10^{-10} torr. The MBD amorphous-Si layer was formed on an oxide layer formed on a Si substrate by room temperature MBD-Si at a rate of 0.5 nm/s. The pressure rose to no more than 10^{-8} torr during deposition. The LPCVD amorphous Si films were deposited using He-diluted SiH_4 (20 percent) gas at 130 Pa and 550° C (measured at the wafer surface by using an infrared thermometer). The base pressure of the LPCVD equipment is 1×10^{-6} torr. After either of these amorphous Si films were exposed to the air, the native oxides were removed by dipping in a dilute HF solution. Amorphous-Si electrodes were annealed in a high-vacuum annealer in which the process pressure was 1×10^{-7} torr. The annealing temperature at the wafer surface was measured by using an infrared thermometer.

The surface morphologies of the deposited Si films were observed by scanning electron microscopy (SEM), and film crystallization was investigated by cross-sectional transmission electron microscopy (TEM). The impurity content in the Si films was analyzed by secondary ion mass spectrometry (SIMS) using cesium-ion bombardment.

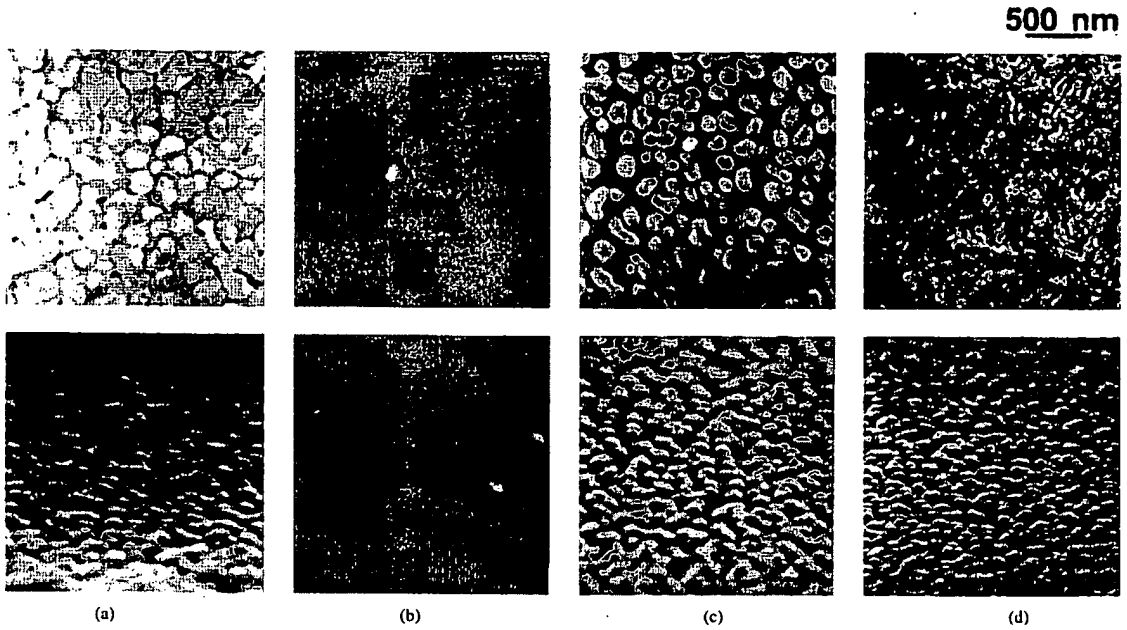


Fig. 1. SEM micrographs of Si film surface morphology after high vacuum annealing. (a) MBD-Si. (b) MBD-Si exposed to air. (c) MBD-Si exposed to air and dipped in HF solution. (d) LPCVD-Si exposed to air and dipped in HF solution.

B. Capacitor Formation Process

Flat amorphous-Si films were deposited by LPCVD at 550°C on SiO_2/Si substrates with contact hole structure. To make storage electrodes, the amorphous-Si film was patterned by lithography and reactive ion etching (RIE). Native oxides on the amorphous-Si electrodes were removed by dipping in a diluted HF solution. HSG-Si surfaces were formed by annealing the amorphous-Si electrodes at 600°C in a high-vacuum annealer. The Si-electrodes with HSG-Si surfaces were doped, using $POCl_3$ gas, by thermal diffusion of phosphorus. SiO_2/Si_3N_4 double-layer films with a SiO_2-equivalent thickness of 7 nm were formed as capacitor dielectric films on the electrode (SiO_2/Si_3N_4/poly-Si structure). Upper electrodes of poly-Si were deposited by LPCVD at 600° C, and this was followed by thermal phosphorus diffusion using $POCl_3$ gas.

The surface area of the deposited Si films was estimated by measuring the capacitance values of stacked capacitors, and the reliability of the capacitors was evaluated in terms of the characteristics of leakage current and the distribution of breakdown fields.

III. Results and Discussions

A. HSG-Si Formation Using High-Vacuum Annealing

Fig. 1 shows top-view and side-view (60° incline) SEM micrographs of Si films annealed under a high vacuum. The surface of the film formed by MBD and subsequent *in-situ* annealing was entirely covered by HSG-Si, Fig. 1(a). As shown in Fig. 1(b), a completely flat surface was observed even on the MBD-Si film that had been exposed to air before annealing. The HSG-Si density on the surface shown in Fig. 1(c) is low. This annealed MBD-Si film was exposed to air and the native oxide was removed before annealing. As shown in Fig. 1(d), however, the entire surface of a film similarly treated but deposited by LPCVD rather than MBD appears to be covered with HSG-Si. The heights of the grain centers (above the foot of the grains) for the samples shown in parts (a), (b), (c), and (d) are, respectively, about 70, 0, 60, and 60 nm.

Fig. 2 shows a cross-sectional TEM micrograph of a HSG-Si film formed by MBD and subsequent *in-situ* annealing. The HSG-Si protrudes from the original amorphous-Si plane, and the amorphous Si surface sinks in around the HSG-Si.

Fig. 3 shows the results of SIMS analysis for Si films. Figs. 3(a) and 3(b) show the impurities in MBD Si and LPCVD Si films exposed to air. The MBD Si film contains many impurities, such as hydrogen, oxygen, and nitrogen. The LPCVD film, on the other hand, contains far fewer impurities. We think this is because the MBD amorphous Si film has many dangling bonds, due to the room temperature deposition and no hydrogen termination, but that dangling bonds of LPCVD amorphous Si, which was deposited at 550°C using SiH_4 gas, are terminated by hydrogen [14], [15]. Hydrogen termination on a silicon surface suppresses native oxide formation in air and even in water for extended periods of time [16]–[18]. It is considered that the difference between the contamination levels for MBD and LPCVD Si films depends on the hydrogen termination of dangling bonds at the surface and in the amorphous-Si film.

It has been reported that HSG-Si is formed on clean amorphous-Si surfaces by migration of surface Si atoms and

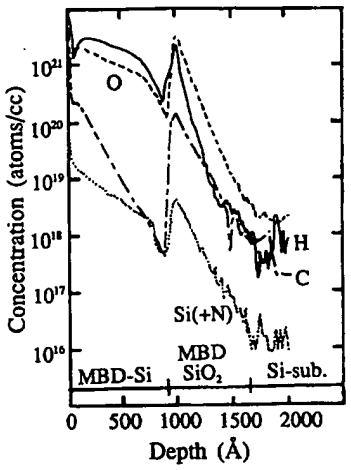
Fig. 2. Cross-sectional TEM micrograph of a HSG-Si film.

crystallization of surface regions [11], [12]. The same group also reported that amorphous Si films with native oxide maintained a completely flat surface during annealing. They argued that the native oxide on amorphous Si surfaces suppresses Si atom migration therefore suppresses the HSG-Si formation.

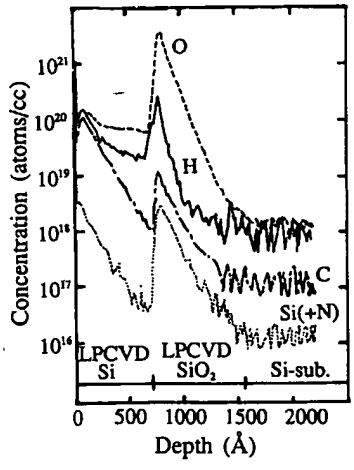
The results shown in Figs. 1 and 3 indicate that the surface morphology of an annealed Si film depends on the level of contamination in the Si film. The HSG-Si density on the MBD-Si film is in fact lower than that on the less contaminated LPCVD-Si film. These results show that the LPCVD amorphous Si film is suitable for HSG-Si fabrication because it is relatively uncontaminated.

These results also show that the high-vacuum annealing method for HSG-Si fabrication does not require the strict temperature control necessary for the LPCVD method [11]. The mechanism of HSG-Si formation is as follows. At the initial step, the nuclei are formed on the amorphous-Si surface due to thermal energy, when the amorphous-Si with a clean surface is heated over the nucleation temperature. The nuclei grow by capturing migrating Si atoms on the amorphous-Si surface during annealing. During high-vacuum annealing, HSG-Si will therefore form when the temperature rises above the nucleation temperature. This is because the nucleation temperature is lower on the amorphous-Si surface than inside the amorphous-Si film [12]. A previous paper showed that the HSG-Si density and size depend on the annealing temperature [11]. Although HSG-Si grains appear on the amorphous-Si surface at 580°C, it takes 30 minutes to get high density HSG-Si on this surface, at this temperature. High-density HSG-Si can be formed within 1 min., however, when amorphous-Si is heated above the 600°C mark. In the case of the LPCVD method, as deposited poly-Si films with a columnar structure are formed for a deposition temperature above 600°C [11]. Therefore, HSG-Si is not formed above 600°C. Strict temperature control is thus necessary for LPCVD HSG-Si formation.

The SEM photographs in Fig. 4 show examples of the capacitor electrode surface morphology. Two types of amorphous-Si storage electrodes with even surfaces, a conventional one and a cylindrical one, were annealed in a vacuum. After annealing, HSG-Si covered the entire surfaces of both types, including the inside walls of cylinders and any side walls which had previously been dry-etched. These results show that the surfaces of all types storage electrodes made of amorphous Si can be covered with HSG-Si by using the high-vacuum annealing process.



(a)



(b)

Fig. 3. Impurity profiles in Si films that were exposed to air. (a) MBD-Si films. (b) LPCVD-Si film.

B. Electrical Characteristics of Capacitors with HSG-Si Storage Electrodes

The surface areas of the storage electrodes were estimated by measuring the capacitance of stacked capacitors with and without HSG-Si on their surfaces. The dielectric films on the storage electrodes were SiO_2/Si_3N_4 dielectric films with a SiO_2-equivalent thickness of 7 nm. The ratio of surface area

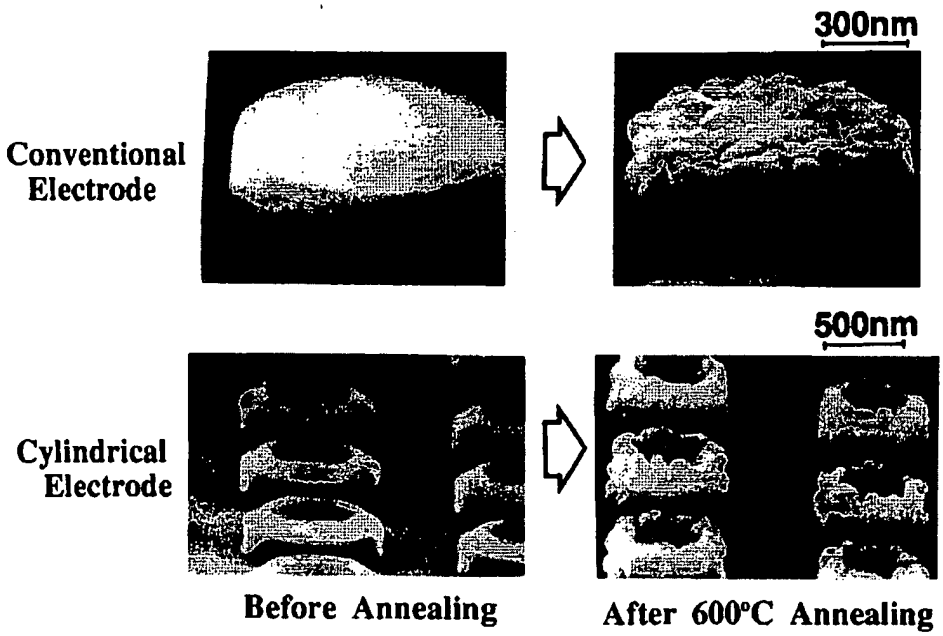


Fig. 4. SEM micrographs of two types storage electrodes before and after high-vacuum annealing at 600° C.

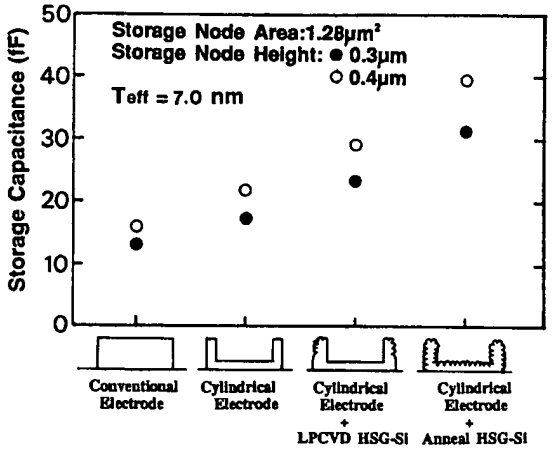


Fig. 5. Storage capacitances for various electrode structures for 64-Mbit DRAM.

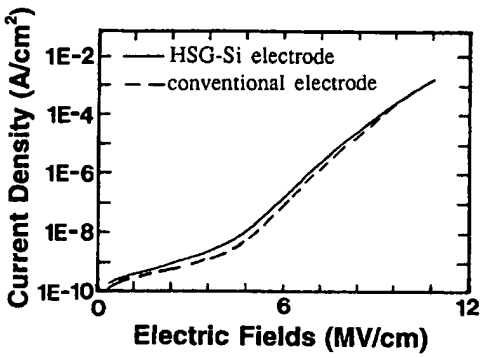


Fig. 6. I-E characteristics of SiO_2/Si_3N_4 dielectric films (T_{eff} = 7 nm) formed on conventional electrodes and on HSG-Si electrodes produced by the proposed high vacuum annealing.

enlargement due to HSG-Si formed by high-vacuum annealing was 1.8. This fact coincides with the fact that the area of the surface covered with hemispheres is approximately 1.8 as large as that of the flat surface, corresponding to the area enlargement for the HSG-Si film with a surface shown in Fig. 2.

Fig. 5 shows storage capacitance estimates for four types of stacked capacitors. Their sizes and dielectric film SiO_2-equivalent thicknesses are defined so as to be suitable for practical 64-Mbit DRAM's. The LPCVD method cannot form HSG-Si on the inner walls and at the foot of the outside walls. The high-vacuum annealing method, in contrast, can produce cylindrical electrodes entirely covered with HSG-Si and therefore with large surface areas. A sufficiently high capacitance, 40 fF, can be achieved with a cylindrical electrode covered with HSG-Si formed by the high-vacuum annealing method, which is clearly enlarges electrode surface area more than the LPCVD method does.

Fig. 6 shows the current-electric field characteristics of SiO_2/Si_3N_4 composite films formed on HSG-Si electrodes made by the proposed annealing method and on conventional polycrystalline Si electrodes. The leakage current increase caused by HSG-Si unevenness is evidently negligibly small.

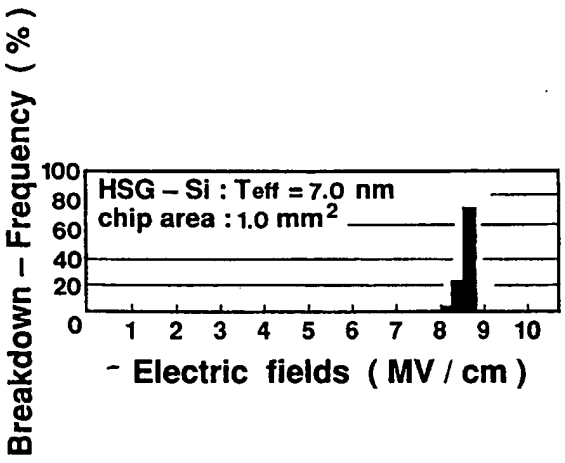


Fig. 7. Breakdown field distribution of SiO_2/Si_3N_4 films (T_{eff} = 7 nm) on HSG-Si electrodes produced by high vacuum annealing.

Fig. 7 shows the distributions of breakdown fields for dielectric films formed on HSG-Si electrodes made by the annealing method proposed here. The peak of the breakdown-field distribution is sharp and no breakdown failure is observed at low electric fields. These results indicate that a low defect density can be obtained on HSG-Si electrodes.

IV. Conclusion

We have developed a new technology for producing high-capacitance storage electrodes by using a new process for forming uneven electrode surfaces of HSG-Si. This fabrication method consists of easily controllable processes: formation of smooth-surface LPCVD amorphous-Si electrodes, removal of native oxide, and high-vacuum annealing. This HSG-Si fabrication method is greatly superior to the previously reported HSG-Si fabrication method, which needs strict temperature control during LPCVD and which cannot form HSG-Si over the entire surface of electrodes. The new process can cover the surfaces of all types of storage electrodes with HSG-Si, increasing their surface areas by a factor of 1.8. Such an increase makes it possible to reduce the height of storage electrodes by using a relatively thick, and therefore more reliable, dielectric film. This technique is applicable to the fabrication of 64-Mbit and larger DRAM's.

V. Acknowledgments

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Hirohito Watanabe received the M.S. degree in material engineering from Tsukuba University, Japan, in 1987.

He joined NEC Corporation in 1987 and is now assistant manager of the Microelectronics Research Laboratories. He has been engaged in the research and development of MOS memory process technology.

He is a member of the Japan Society of Applied Physics.

Toru Tatsumi received the M.S. degree in physics from Waseda University, Japan, in 1983.

He joined NEC Corporation in 1983 and is now assistant manager of the Microelectronics Research Laboratories. He has been engaged in the research and development of Si-MBE.

He is a member of the Japan Society of Applied Physics.

Akira Sakai received the M.S. degree in metallurgical engineering from Nagoya University, Japan, in 1986.

He joined NEC Corporation in 1986 and is now assistant manager of the Microelectronics Research Laboratories. His principal work is the characterization of semiconductor materials by transmission electron microscopy.

He is a member of the Japan Society of Applied Physics.

Taeko Ikarashi graduated from Kyoritu College, Japan, in 1987.

She joined NEC Corporation in 1987 and is now a member of the Microelectronics Research Laboratories. She has been engaged in the research and development of Si-MBE.

She is a member of the Japan Society of Applied Physics.

Nahomi Aoto received the Dr. degree in material engineering from Tsukuba University, Japan, in 1991.

She joined NEC Corporation in 1983 and is now manager of the Microelectronics Research Laboratories. She has been engaged in the research and development of Si LSI process technology.

She is a member of the Japan Society of Applied Physics.

Takamaro Kikkawa (S'74–M'76) was born in Shimane, Japan, in 1952. He received the B.S. and M.S. degrees in electronic engineering from Shizuoka University, Shizuoka, and the Ph.D. degree in electronic system from the Tokyo Institute of Technology, Tokyo, in 1974, 1976, and 1994, respectively.

In 1976, he joined NEC Corporation, Japan, and has been engaged in the development of devices and processes for integrated circuits. From 1983 to 1984, he was a Visiting Scientist at the Massachusetts Institute of Technology, Cambridge, where he worked on thin-film transistors under Prof. Dimitri A. Antoniadis. He is currently the Senior Manager of Thin Film Process Development Laboratory, ULSI Device Development Laboratories.

Dr. Kikkawa is a member of the Electrochemical Society and the Japan Society of Applied Physics.